IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND-ODESSA DIVISION

REDSTONE LOGICS LLC, Plaintiff, v. NXP USA, Inc., Defendant.	Case No. 7:24-cv-00028-DC-DTG JURY TRIAL DEMANDED

DEFENDANT NXP USA, INC.'S OPENING CLAIM CONSTRUCTION BRIEF

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C	U.S. Patent No. 7,538,625 (*Cesky*)
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[1] Exhibits A through H are exhibits to the December 3, 2024 Declaration of Dr. John Villasenor In Support of NXP's Opening Claim Construction Brief (Ex. 1).

I. INTRODUCTION

The Asserted Claims of U.S. Patent No. 8,549,339 (the "'339 Patent")[2] generally relate to a "multi-core processor" where first/second "set[s] of processor cores" are each "configured to dynamically receive" a corresponding first/second "clock signal" and "supply voltage." *See,* e.g., '339 Pat., Cl. 1. But the claims do not generally cover any such arrangement. In order to obtain allowance, each asserted independent claim was amended to further require that "the first clock signal ***is independent*** from the second clock signal" (the "Independent Term").

Before and after the '339 Patent, there were multiple known ways to generate the various clock signals provided to various groups of components in a microprocessor. First, a ***single*** reference oscillator approach provides multiple clocks derived from and ***dependent on*** the same reference oscillator source, either by simply distributing that source to multiple clock lines or by dividing or multiplying the frequency of that reference oscillator source to create multiple clock rates. The examiner rejected the '339 Patent's original claims over this approach. Second, a ***multiple*** reference oscillator approach—the sole approach disclosed in the '339 Patent—provides multiple clock signals ***not dependent*** on the same reference oscillator.

The applicant, in no uncertain terms, distinguished the ***single*** reference oscillator approach from the Independent Term in statements made during prosecution. NXP's construction is taken ***word-for-word*** from those statements. These statements confirm the plain and ordinary meaning and, while not necessary, also meet the standard for a clear and unmistakable disavowal of claim scope.

[2] The '339 Patent is Dkt. 1-1 and is also attached as Ex. A to the December 3, 2024 Declaration of Dr. John Villasenor In Support of NXP's Opening Claim Construction Brief.

The Asserted Claims are also invalid due to their use of indefinite claim language. First, as mentioned above, the claims recited that sets of processor are "***configured to dynamically receive***" a first/second "supply voltage" and "output clock signal," but it is entirely unclear how a processor can be "configured" as such.[3] Second, certain dependent Asserted Claims describe the location of structures using terms that do not refer to any particular location or provide any guidance on the metes and bounds of any such region (i.e., "in a ***periphery*** of the multi-core processor" and "in a ***common region*** that is ***substantially central*** to the first set of processor cores and the second set of processor cores").

II. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art ("POSITA") at or around the relevant time of the alleged invention would have had at least a Bachelor's degree in electrical engineering, computer engineering, computer science, or a similar field, as well as at least 2 years of academic or industry experience designing or analyzing electronic circuits, semiconductors, processors, or power management, and related firmware and software, or the equivalent. A POSITA with a higher level of education may have fewer years of academic or industry experience, or vice versa. Ex. 1, Declaration of Dr. John Villasenor Regarding Claim Construction ("Villasenor Decl.") at ¶ 25.

III. OVERVIEW OF THE '339 PATENT

The '339 Patent relates to an arrangement of clock and voltage sources to different groups of processor cores in a multi-core processor. '339 Patent at Abstract; 1:61-2:40. The '339 Patent explains that prior art multi-core processors required that "[e]ach processor core in a conventional multi-core processor generally shares the same supply voltage and clock signal to simplify the interfaces between the processor cores." '339 Patent at 1:7-14. To that end, the '339 Patent

[3] Unless otherwise indicated, all emphasis is added.

proposes that each processor core group has an independent power profile powered with a separate supply voltage and that each processor core group obtain a clock output signal from a phase locked loop (PLL) that receives a clock input signal from an "independent clock domain." *Id.* at 2:27-31, 4:1-17, Fig. 3.

This approach is illustrated below in annotated Fig. 3 of the '339 Patent, which depicts three independent clock signals, "the clock signal 1, the clock signal 2, the clock signal 3" (annotated in green), providing independent inputs to "the respective phase lock loops (PLLs)" 1, 2, and 3. *Id.* at 4:1-17, Fig. 3.

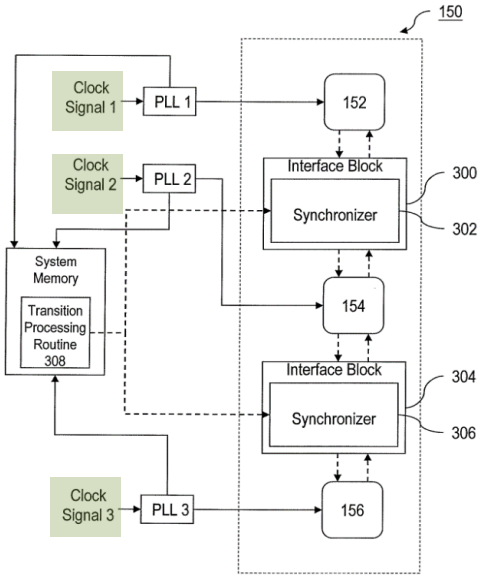


FIG. 3

Id., Fig. 3 (annotated).

Consistent with Fig. 3, each asserted independent claim (Claims 1 and 21) of the '339 Patent recites "a first phase lock loop (PLL) having a first clock signal as input" and "a second PLL having a second clock signal as input" wherein "the first clock signal is independent from the second clock signal." *Id.* at Claims 1 and 21.

IV. DISPUTED TERMS REQUIRING CONSTRUCTION

A. Term 1: "the first clock signal is independent from the second clock signal"

'339 Patent Claim(s)	Redstone's Proposed Construction	Defendant's Proposed Construction
Claims 1, 21	Plain and ordinary meaning	Plain and ordinary meaning, where the plain and ordinary meaning requires that the first and second clock signals are provided by or processed (i.e., divided or multiplied) from different reference oscillator clocks.

A dispute exists because Redstone has (a) refused to stand by the prosecution history statements reflected in NXP's construction and (b) contended in its infringement contentions, inconsistent with these statements, that the claims may be met by two different clock sources derived from a single "crystal using the internal oscillator amplifier." *See*, e.g., Ex. 2, Infringement Contentions at 27-28. Thus, the dispute between the parties is whether the phrase "the first clock signal is independent from the second clock signal" is broad enough to encompass a "first clock signal" and "second clock signal" that are derived from the same reference oscillator clock. NXP's construction, which is taken word-for-word from the applicant's prosecution history statements, implements both the plain meaning and the applicants' clear and unmistakable disavowal of claim scope and confirms that the first and second clock signals cannot be derived from the same reference oscillator clock.

1. The plain claim language and specification require a specific approach to providing clock signals in multicore processors

Each core in a multicore processor requires a clock timing reference to operate. Villasenor Decl. at ¶ 35. The basic design principles generating and distributing clock signals in a multicore processor were widely known at the time the '339 Patent was filed. *Id.* at ¶ 36. Two known approaches are relevant to this dispute. *Id.* at ¶¶ 36-42, 47-52. Both known approaches begin with the understanding that clock signals typically originate from one or more external reference oscillator clocks. *Id.* The first such approach uses a ***single*** reference oscillator clock. For example, one prior art reference, *Jacobowitz*,[4] illustrates a reference clock signal (V_R) (red) from the master reference oscillator (112) (blue) that is then distributed through local oscillators (108) (green) to various processor cores and used by each core. *See Jacobowitz* at ¶¶ [0037]-[0038].

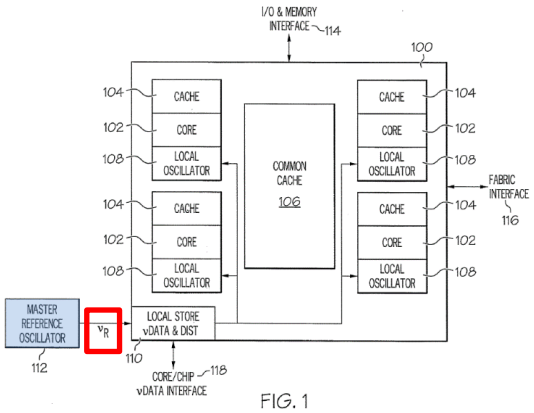


FIG. 1

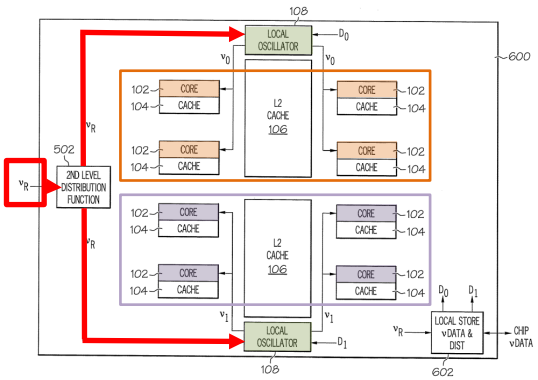


FIG. 6

Jacobowitz at Figures 1 and 6 (annotated).

Another prior art reference, *Kim*,[5] discloses, once again, a clock distribution network of a multi-core processor having a single reference oscillator clock source 170/270 (blue) in two

[4] *Jacobowitz* is listed on the face of the patent and thus constitutes intrinsic evidence. *See V-Formation, Inc. v. Benetton Group SPA*, 401 F.3d 1307, 1311 (Fed. Cir. 2005).

[5] *Kim* is likewise listed on the face of the patent and thus constitutes intrinsic evidence. *See V-Formation, Inc.*, 401 F.3d at 1311.

different embodiments. *Kim* at ¶¶ [0024]-[0025], Figs. 1-2 (annotated below). But, in the case of *Kim*, that single reference oscillator clock source passes through a main PLL 160/260 (green) that includes "one or more frequency dividers" that can modify the reference clock source rate to be a multiple of the original clock rate. *Id. Kim*'s main PLL 160/260 enables clock signals at multiple clock rates, but all signals are still ***dependent*** on the same/single reference oscillator clock 170/270. Villasenor Decl. at ¶¶ 51-52. Thus, in both *Jacobowitz* and *Kim*, a change to the single reference oscillator clock will impact the clock signal delivered to each core, demonstrating those clock signals share a dependency. *Id.*

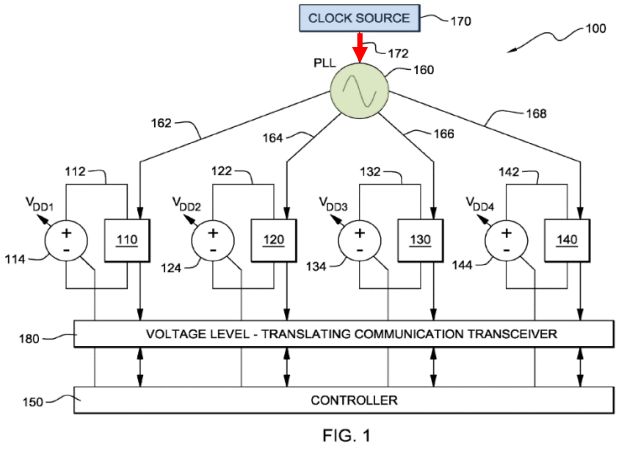


FIG. 1

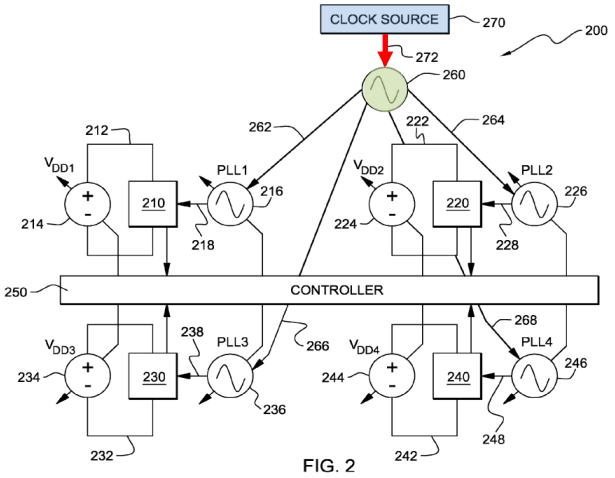


FIG. 2

Kim at Figures 1 and 2 (annotated).

The second approach to generating and distributing clock signals employs ***multiple*** clock sources (e.g., reference oscillator clocks). The '339 Patent discloses and claims this second approach. For example, Fig. 3 of the '339 Patent illustrates a clock distribution network that, rather than using a single common source (e.g., reference oscillator clock), employs three independent sources—"the clock signal 1, the clock signal 2, the clock signal 3" (annotated in green)—that feed "the ***respective*** phase lock loops (PLLs)" 1, 2, and 3 and, in turn, ***respective*** processor cores 152, 154, 156. *Id.* at 4:1-17, Fig. 3; *see also id.* at 1:7-10.

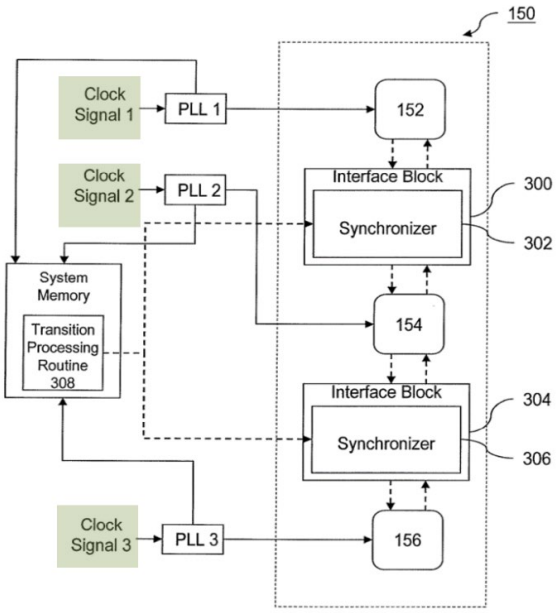


FIG. 3

Id., Fig. 3 (annotated). In contrast to *Kim*'s single reference oscillator approach, in the multiple clock source approach, "clock signal 1" that feeds core 152 does not share the same common clock source that also provides "clock signal 2." The clock signal delivered to core 154, fed from "clock signal 2," is ***independent*** from "clock signal 1."

Accordingly, the plain claim language "the first clock signal is ***independent*** from the second clock signal" is consistent with this multiple reference oscillator clock approach—the only approach disclosed in the '339 Patent—and inconsistent with the single reference oscillator clock approach.

2. The prosecution history confirms that the Asserted Claims do not claim two clock signals derived from a single reference oscillator clock

To the extent there was any doubt that the plain claim language requires that the first and second clock signals be provided by or processed (i.e., divided or multiplied) from ***different*** reference oscillator clocks, the file history is conclusive. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1317 (Fed. Cir. 2005) (*en banc*) ("the prosecution history can often inform the meaning of

the claim language by demonstrating how the inventor understood the invention"). During prosecution, the examiner rejected the then-pending claims over the two examples of the single reference oscillator approach, *Jacobowitz* and *Kim*, discussed above. *See* Ex. F[6] at 4-9 (Office Action (Aug. 29, 2012)). In response, the applicant argued that *Jacobowitz* "disclosed using ***a single reference clock***," which was different than FIG. 3 of the '339 Patent where "clock signals 1 through 3 were ***different/independent clock signals*** input to the PLLs." *See* Ex. G at 2 (Examiner Interview (Nov. 27, 2012)). "The examiner agreed that Jacobowitz discloses using ***a single reference clock***," but disagreed the current claims excluded such an arrangement. *Id*. "Applicant's representative stated that he would discuss amends [sic] to the claims." *Id.*

Two days later, the applicant filed a response amending the independent claims to add the phrase "the first clock signal ***is independent*** from the second clock signal." *See* Ex. H at 3, 5-7 (Applicant's Resp. (Nov. 29, 2012)). In characterizing why *Jacobowitz* and *Kim* were contrary to that new claim language, the applicant used the precise language in NXP's construction:

References do not meet claim because …	**NXP's Construction**
"Jacobowitz discloses using a **single** reference clock"—the "system reference oscillator clock"—"distribute[d]" to all cores	the first and second clock signals are provided by or processed (i.e., divided or multiplied) from **different** reference oscillator clocks
"Kim discloses … having a **single** clock source … then processed (i.e., divided or multiplied) and provided to each of the cores."	

[6] As used herein, Exhibits A-H are the exhibits to the December 3, 2024 Declaration of Dr. John Villasenor In Support of NXP's Opening Claim Construction Brief.

First, the applicant asserted that "Jacobowitz fails to disclose or teach . . . the first clock signal is ***independent*** from the second clock signal" based on *Jacobowitz* disclosing "the microprocessor chip (e.g., 600) receiv[ing] a system reference oscillator clock frequency (V_R) and distribut[ing] V_R to local oscillators 108." Ex. H at 9-10. The applicant thus made clear that "using a ***single*** reference clock"—the "system reference oscillator clock"—for the first and second clock signals cannot meet the requirement that "the first clock signal is ***independent*** from the second clock signal." *Id.*; Ex. G at 2; *see also* Ex. H at 11 ("neither Jacobowitz nor Kim discloses having sets of processor cores configured to receive multiple ***and independent*** clock signals.").

Second, the applicant explained that *Kim* does not disclose having a "first clock signal [that] ***is independent*** from the second clock signal" but:

> ***[i]nstead,*** Kim discloses the apparatus comprising a multi-core processor (i.e., 100 in FIG. 1 or 200 in FIG. 2) having ***a single clock source*** (i.e., 170 in FIG. 1 or 270 in FIG. 2). The clock signal from this single clock source is then ***processed (i.e., divided or multiplied)*** and provided to each of the cores. *See Kim* at ¶¶ [0024]-[0025] and FIGs 1 - 2.

See Ex. H at 10-11 (Applicant's Resp. (Nov. 29, 2012)).

Thus, it is not enough to meet the plain language of "independent" to have multiple clock signals with different rates or that one of the clock signals may be changed by "process[ing]" a common source—to be independent there must be ***different clock sources (i.e., reference oscillator clocks)***. The applicant again confirmed this by arguing "neither *Jacobowitz* nor *Kim* discloses having sets of processor cores configured to receive ***multiple and independent*** clock signals." Ex. H at 11. By referring to "multiple and independent," the applicant confirmed that "independent" must be more than "multiple." *See id.* Accordingly, a POSITA would understand the plain and ordinary meaning of "***independent***" as used the '339 Patent requires that the first and second clock signals are provided by or processed (i.e., divided or multiplied) from ***different***

reference oscillator clocks. This plain and ordinary meaning excludes multiple clock signals "processed (i.e., divided or multiplied)" from a ***single*** clock source (e.g., clock source 170 or 270, which may be "a crystal oscillator"). Villasenor Decl. at ¶¶ 33, 53-54.

Because these passages confirm the plain and ordinary meaning, it is not necessary for them to meet the standard for a clear and unmistakable disavowal of claim scope—but they also meet the standard for disavowal. "'Prosecution disclaimer can arise from both claim amendments and arguments.' Here, we have both." *SpeedTrack, Inc. v. Amazon.com*, 998 F.3d 1373, 1379 (Fed. Cir. 2021) (internal citation omitted) (quoting *Tech. Props. Ltd. LLC v. Huawei Techs. Co., Ltd.*, 849 F.3d 1349, 1357 (Fed. Cir. 2017)). As discussed above, the applicant repeatedly distinguished art "using ***a single reference clock***," first pointing to the specification and then, when the examiner insisted, amending the claims and pointing to that added language. *See* Ex. G at 2, Ex. H at 3, 5-7. In no uncertain terms the applicant contrasted ("***[i]nstead***") the claim language "first clock signal [that] ***is independent*** from the second clock signal" with prior art "having ***a single clock source***" and that is "***processed (i.e., divided or multiplied)*** and provided to each of the cores." Ex. H at 10-11. "The applicant[] in this case must be understood to have been distinguishing their invention (as newly narrowed by the added limitation) on the basis of [that] distinction." *Sound View Innovations, LLC v. Hulu, LLC*, 33 F.4th 1326, 1334 (Fed. Cir. 2022). To permit the claims to cover single clock arrangements "even though [the cited art] discloses that exact arrangement" "leads to [a] paradoxical result." *SpeedTrack*, 998 F.3d at 1380. "That can't be right." *Id.* "They are disclaimed." *Id.* at 1379.

B. Term 2: "each processor core from the first/second set of processor cores is configured to dynamically receive a first/second supply voltage [from a power control block] and a first/second output clock signal"

'339 Patent Claim(s)	Redstone's Proposed Construction	Defendant's Proposed Construction
Claims 1, 21	Plain and ordinary meaning	Indefinite

The term "each processor core from the first/second set of processor cores is configured to dynamically receive a first/second supply voltage [from a power control block] and a first/second output clock signal" is indefinite because it fails to inform a POSITA, with reasonable certainty, of how a processor core can be "configured to dynamically receive" a supply voltage and an output clock signal. *See Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). While four variants of this phrase appear in the '339 Patent's asserted claims, they distill to: "each processor core…is ***configured to dynamically receive*** a [] supply voltage […] and a [] output clock signal."

Redstone contends this phrase should be understood according to its plain and ordinary meaning, however, Redstone has not sought to clarify the scope of the purported plain and ordinary meaning. As confirmed by the declaration of Dr. John Villasenor, the sub-phrase "'configured to dynamically receive' . . . does not have a common understanding in the relevant field." *See* Villasenor Decl. at ¶ 61. And, the '339 Patent's claims and specification do not resolve the ambiguity. *Id.*

Beginning with the language of the claims themselves, the indefiniteness arises from the inclusion of "dynamically," a vague term that the patent never defines and that has no fixed meaning in the art. *See* Villasenor Decl. at ¶¶ 63-65. Processor cores commonly receive supply voltages and clock signals. *Id.* at ¶ 63 (noting "a typical processor core is capable of receiving signals, including voltages and clock signals" and this "common attribute of processor cores [] is required for them to function"). Significantly, Claim 5—which depends from independent

Claim 1—reflects the common behavior, as the claim requires that the "set of processor cores are ***configured to receive*** one or more control signals." Unlike the independent claim from which it depends, Claim 5 does not require dynamically receiving anything, demonstrating that the patentee knew how to claim common processor behavior when that was the intent. *See id.* at ¶ 63.

Because the bounds of "dynamically" are not specified, Redstone's plain and ordinary meaning construction invites the Court to read the ambiguous word "dynamically" out of Claims 1 and 21 altogether, but it is hornbook claim construction law that a court must "give meaning to all the words in [the] claims." *Exxon Chem. Patents, Inc. v. Lubrizol Corp.*, 64 F.3d 1553, 1557 (Fed. Cir. 1995), *rev'd on other grounds*, 137 F.3d 1475, 1484 (Fed. Cir. 1998) (citing *In re Sabatino*, 480 F.2d 911, 913 (C.C.P.A. 1973) ("Claim limitations defining the subject matter of the invention are never disregarded.")).[7]

The '339 Patent's specification does not resolve the ambiguity. The specification is silent regarding a processor core's dynamic receipt of a voltage or clock, much less how to "configure[]" a processor core to "dynamically receive" anything. *See* Villasenor Decl. at ¶¶ 63-65. Indeed, the specification never uses the word "dynamically," and its root "dynamic" only appears twice in contexts unrelated to the phrase at issue. *Id.* First, in the high-level "Background of the Disclosure," the '339 Patent specification mentions "dynamic supply voltage and clock speed control" in the context of "power consumption management." '339 Patent at 1:10-14; *see also* Villasenor Decl. at ¶ 66. But power consumption management is distinct from the dynamic receipt

[7] "Allowing a patentee to argue that physical structures and characteristics specifically described in a claim are merely superfluous would render the scope of the patent ambiguous, leaving examiners and the public to guess about which claim language the drafter deems necessary to his claimed invention and which language is merely superfluous, nonlimiting elaboration." *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006). "For that reason, claims are interpreted with an eye toward giving effect to all terms in the claim." *Id.*

of a supply voltage and an output clock signal by a processor core, let alone the configuration of the processor core to enable such dynamic receipt. Villasenor Decl. at ¶ 66. Second, the specification describes "dynamically adjusting the power profile for a stripe in response to changes in computational requirements" in the context of Figure 1. '339 Patent at 3:17-20; *see also* Villasenor Decl. at ¶ 67. But, this disclosure concerns power profile adjustments carried out by the control blocks, again saying nothing about the dynamic receipt of a voltage and clock signal by a processor core, or how to configure the processor core to permit such dynamic receipt. Villasenor Decl. at ¶ 67.

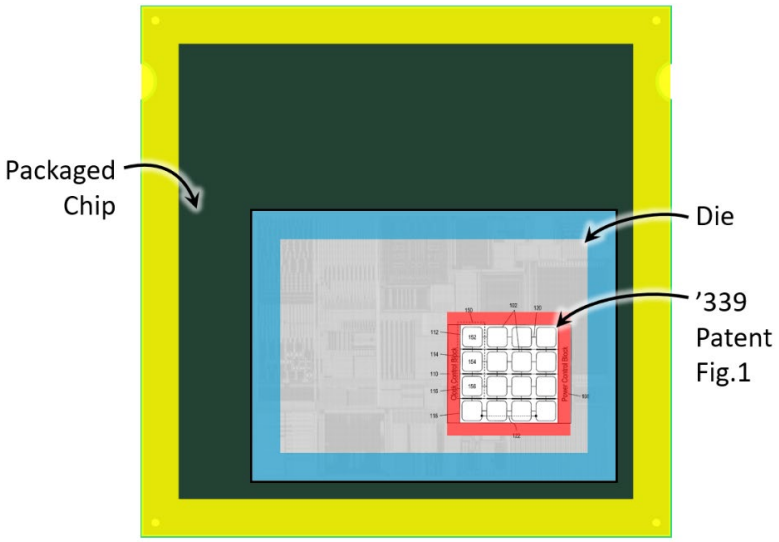
Ultimately, there is nothing within the '339 Patent or the knowledge of one skilled in the art that informs with reasonable certainty what differences distinguish (a) a set of processor cores that is configured to dynamically receive a supply voltage and clock signal with (b) one that is not configured to dynamically receive such signals. *See id.* at ¶ 68. For that reason, the phrase "each processor core from the first/second set of processor cores is configured to dynamically receive a first/second supply voltage [from a power control block] and a first/second output clock signal" is indefinite.

C. Term 3: "located in a periphery of the multi-core processor"

'339 Patent Claim(s)	**Redstone's Proposed Construction**	**Defendant's Proposed Construction**
Claim 5	Plain and ordinary meaning	Indefinite

The term "located in a periphery of the multi-core processor" is indefinite because it fails to inform a POSITA, with reasonable certainty, when a component is "located in a periphery of the multi-core processor" and when it is not. *See Nautilus*, 572 U.S. at 901. The inclusion in Claim 5 of "periphery" leads to ambiguity in two respects, neither of which is resolved by the patent's claims, the specification, nor the knowledge of a person of skill in the art.

First, the scope of a "multi-core processor" is unclear. In order to determine whether a "control block[]" is "located in the periphery of the multi-core processor," as Claim 5 requires, one must identify the physical bounds of the multi-core processor. The term "multi-core processor" does not have a fixed meaning in the art, but instead is applicable at multiple levels of granularity. *See* Villasenor Decl. ¶ 74 (noting that multi-core processor in Claim 5 "might refer to multiple things"); *id*. at ¶ 76 (describing possibilities for a multi-core processor within the scope of Claim 5). A person of skill in the art might interpret the term "multi-core processor" in different ways: as the individual processor cores, as the complete semiconductor die containing the processor cores and additional necessary circuitry, or as the packaged die encased in plastic and connected to electrical contacts. *Id*. at ¶ 76. Each interpretation leads to different boundaries for defining the multi-core processor's "periphery," as depicted below:



Villasenor Decl., Figure B.

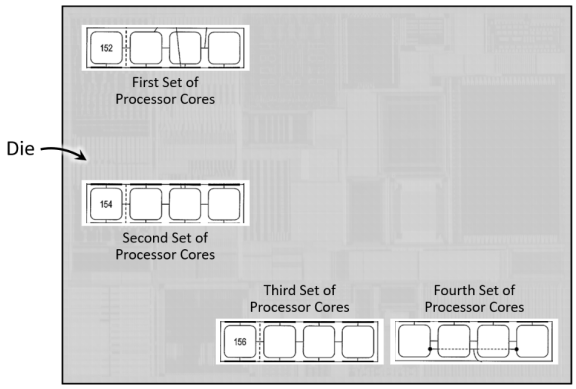
Second, even if the applicable scope and boundary of a multi-core processor was ascertainable in light of the claims, "periphery" is a term of degree—how close to the boundary of the multi-core processor must the claimed control blocks be located in order to be considered

"located in a periphery"? *See id.* at ¶ 80. The claims do not clarify this, nor does this term of degree have a fixed meaning to one skilled in the art. *See id.*

Turning to the '339 Patent's specification, neither ambiguity presented by the claims is resolved. Regarding the scope of periphery, the specification is silent. "[P]eriphery" appears only once in the specification: "A power profile associated with an individual processor core may be controlled through signals that may be received from ***control blocks that are located in the periphery*** of the multi-core processor." '339 Patent at 1:62-65. This usage of "periphery" merely parrots Claim 5 and offers no additional guidance as to the appropriate scope of periphery. Neither the '339 Patent's claims nor its specification provide a standard by which the scope of the claimed "periphery" may be determined. *See Biosig Instruments, Inc. v. Nautilus, Inc.*, 783 F.3d 1374, 1378 (Fed. Cir. 2015) ("When a 'word of degree' is used, the court must determine whether the patent provides 'some standard for measuring that degree.'" (quoting *Enzo Biochem, Inc. v. Applera Corp.*, 599 F.3d 1325, 1332 (Fed. Cir. 2010)).

Further, the patent's specification does not define the boundary of a multi-core processor in a manner sufficient to identify any associated "periphery." The specification notes that "FIG. 1 illustrates an example configuration of a multi-core processor." '339 Patent at 1:26-27. The above graphic depicting the various understandings of a multi-core processor includes Figure 1 within the red boundary. But, viewing the term "multi-core processor" as merely a collection of processor cores does not resolve the ambiguity presented by the claims. *See* Villasenor Decl. at ¶¶ 81-82.

A person of skill in the art understands that the processor cores in the "multi-core processor" of the Asserted Claims need not be arranged in the grid depicted in Figure 1 of the '339 Patent, but instead may be arranged throughout the semiconductor die, as shown in the example below:



Villasenor Decl., Figure C; *see also id.* at ¶ 81 ("A POSITA would understand that that the processor cores of a multi-core processor need not be located immediately adjacent to one another in the manner depicted in the patent's Figure 1.").

With the sets of processor cores spread throughout the die, as depicted above, a person of skill in the art could not understand with reasonable certainty what constitutes the "periphery" of such a multi-core processor, as *Nautilus* requires. Villasenor Decl. at ¶ 80; *see also Nautilus*, 572 U.S. at 901.

One skilled in the art could not reasonably understand what constitutes the "periphery of the multi-core processor" in the context of the '339 Patent's claims and specification, making it impossible to know whether a control block is "located in a periphery of the multi-core processor;" this phrase is indefinite.

D. Term 4: "located in a common region that is substantially central to the first set of processor cores and the second set of processor cores"

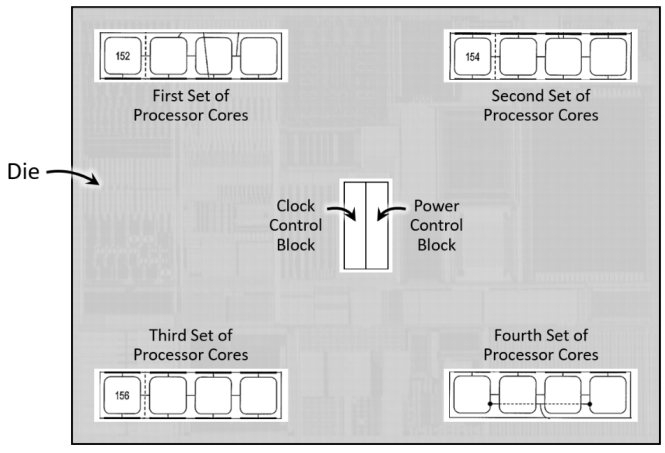
'339 Patent Claim(s)	Redstone's Proposed Construction	Defendant's Proposed Construction
Claim 14	Plain and ordinary meaning	Indefinite

The term "located in a common region that is substantially central to the first set of processor cores and the second set of processor cores" is indefinite because it fails to inform a POSITA, with reasonable certainty, both (1) when a component is "located in a common region,"

or not, and (2) when the "region" is "substantially central to the first set of processor cores and the second set of processor cores," or not. *See Nautilus*, 572 U.S. at 901.

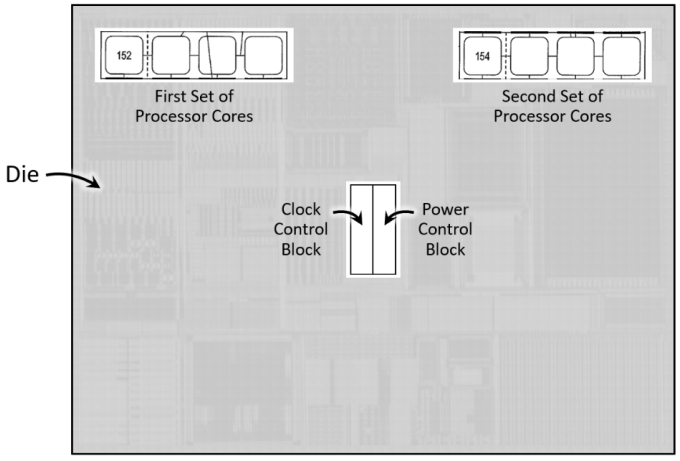
Beginning with the second ambiguity identified above, Claim 14 requires "control blocks located . . . substantially central" to the sets of processor cores. "[S]ubstantially central" is a term of degree that, in the context of the '339 Patent's claims and specification, "fails to provide sufficient notice of its scope." *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1371 (Fed. Cir. 2014) ("As we have explained, a term of degree fails to provide sufficient notice of its scope if it depends 'on the unpredictable vagaries of any one person's opinion.'" (citation omitted)).

Looking first at the claims, independent Claim 1 and dependent Claim 14 provide no physical requirement for the individual processor cores of the claimed multi-core processor. As noted above in Section IV.C, one skilled in the art understands that the components of a multi-core processor may be located throughout the semiconductor die upon which they are typically formed; the processor cores need not be immediately adjacent in the manner shown in Figure 1 of the '339 Patent. *See also* Villasenor Decl. at ¶¶ 81-82. The below figure depicts one possible physical layout of the multi-core processor of the claims, with the sets of processor cores from '339 Patent Figure 1 placed towards the corners of the semiconductor die and the control blocks at the midpoint between the sets of processor cores:



Villasenor Decl., Figure D.

Even in such an arrangement, a person of skill would not know whether the control blocks are "substantially central" by virtue of being equidistant from each set of cores, or whether the control blocks are not substantially central given the separation of the processor cores from the control blocks. *Id.* at ¶ 95. The uncertainty within "substantially central" becomes more pronounced, however, if only two sets of processor cores are considered—as in the Asserted Claims. The figure below depicts the first and second sets of processor cores at the top of the die with control blocks near the middle:



Id., Figure E.

A person skilled in the art would not know in the context of Claim 14 whether (a) the depicted control blocks are "substantially central" because they are at the horizontal midpoint between the first and second sets of processor cores, or (b) whether the control blocks are not "substantially central" because they are not in the same vertical position as the sets of processor cores. *Id.* at ¶¶ 97, 98.

The specification of the '339 Patent similarly provides no guidance regarding the scope of "substantially central." *See Interval Licensing*, 766 F.3d at 1371 ("Where, as here, we are faced with a 'purely subjective' claim phrase, we must look to the written description for guidance."

(citation omitted)). The term "central" and the phrase "substantially central" are never used in the patent's specification. And, while the term "substantially" appears twice, neither use concerns the physical relationship between control blocks and processor cores. *See* '339 Patent at 4:24-27 (denoting commonality between Figs. 3 and 4), 6:56-57 (providing boilerplate regarding "the use of substantially any plural and/or singular terms herein.").

Because Claims 1 and 14, and the patent's specification, do not require a physical arrangement of the sets of processor cores, a person skilled in the art could not determine with reasonable certainty whether or not "control blocks" are "substantially central" to the sets of processing cores. "[L]ocated in a common region that is substantially central to the first set of processor cores and the second set of processor cores" is therefore indefinite.

An independent ground for indefiniteness arises from Claim 14's use of "common region." Claim 14 requires "the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a ***common region***." Though not a model of clarity, a person of skill understands this phrase means the first and second sets of processor cores share a common region where control blocks are located. *See* Villasenor Decl. at ¶ 89. The claims provide no indication, however, of what constitutes a "region" corresponding to a set of processor cores or how such regions could be in "common." *Id.* at ¶¶ 90-91.

While one possible interpretation of a common region shared by first and second sets of processor cores could be that the sets of processor cores "overlap" in physical space, this interpretation conflicts with dependent Claim 9, which depends from Claims 1 and 8. Claim 9 (through its dependencies) requires a "first set of processor cores [] located in a first region," a "second set of processor cores [] located in a second region," and "the first region and the second

region are overlapping regions." When construing claims, "[d]ifferent claim terms are presumed to have different meanings." *SimpleAir, Inc. v. Sony Ericsson Mobile Communs. AB*, 820 F.3d 419, 431 (Fed. Cir. 2016) (citing *Bd. of Regents of the Univ. of Tex. Sys. v. BENQ Am. Corp.*, 533 F.3d 1362, 1371 (Fed. Cir. 2008)). Therefore, "common region" in Claim 14 must mean something other than overlapping, though such other meaning remains unclear. *See* Villasenor Decl. at ¶ 91.

The '339 Patent's specification does not resolve the ambiguity introduced by "common region" in Claim 14. The patent's specification never uses the phrase "common region." And, while the specification describes an embodiment with two control blocks "arranged in a common area," that use is distinct from Claim 14; there is no reference in the specification to sets of processor cores sharing a "common area." *Id.* at ¶ 92.

The phrase "located in a common region that is substantially central to the first set of processor cores and the second set of processor cores" is indefinite for two independent reasons: a person of skill cannot determine with reasonable certainty the scope of each of "common region" and "substantially central."

V. CONCLUSION

For the foregoing reasons, Defendant respectfully requests the Court construe Term 1 as proposed by Defendant and find Terms 2, 3, and 4 indefinite as set forth herein.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing document was served on counsel of record via the Court's electronic filing system on December 4, 2024.

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